The Care and Feeding of High Speed Dividers

Application Note

AN178 - 2.2 March 1994

Circuit design and layout for high speed dividers operating at frequencies up to 5GHz owe much more to analog RF design techniques than normal digital ones and the limitations on flexibility and component choice inherent in UHF RF design are of paramount importance in successful designs.

PRACTICAL DESIGN CONSIDERATIONS

High speed divider applications require the printed circuit boards to be mechanically designed with two considerations in mind:

(1) Electrical performance
(2) Mechanical and thermal performance.

These two considerations are inter-related; for example, the use of 1/16 inch thick fibreglass PC board may be desirable mechanically, but a 50Ω stripline on this thickness of board is about 5/32 inch wide, and is thus too wide to pass between the pins of an IC.

Most of the heat conducted from a dual-in-line IC package is removed from the bottom of the package. Less than 10 % is conducted out by the leads, and because of the cavity between the chip and lid, relatively little through the top of the package.

For this reason, the use of a double-layer PC board layout is recommended, with a ground plane top surface. Where 1/32 inch thick material is used, a top surface ground plane will add substantially to the heat dissipation capabilities of the board

For use at very high frequencies, consideration must be given to the type of component used. Carbon composition resistors are more resistive at high frequencies than either carbon or metal film types, and are available in very small sizes. Bypass capacitors need to be chosen carefully if they are to act as low impedances, as series inductance leads to an increasing impedance with frequency above the series resonant frequency of the device. As a guide, a 1000pF disc ceramic capacitor with 1/4 inch leads will be self resonant at about 75MHz, and will appear as an inductive impedance of about 22Ω at 800MHz. The use of chip capacitors is recommended above 500MHz, although leaded monolithic ceramic capacitors with suitably short leads are often acceptable.

The use of a ground plane for RF decoupling purposes is often recommended, and can be helpful. However, the danger is that the ground current paths in the plane are not defined very well, and because of this lack of definition, the ground plane can cause unsatisfactory operation. Probably the best method is to return all the bypass capacitors to a single point (as in Fig 1) and return this point to the ground plane.

Also note that in Fig.1 the output load resistors have their grounded ends connected together and a common return used Because the currents in the resistors are in antiphase, cancellation of the inductive effects taken place, and the path followed by the relatively large output currents is controlled. Defining the ground current path is more important in applications like frequency synthesis, where a relatively large part of the system may be on one PCB.

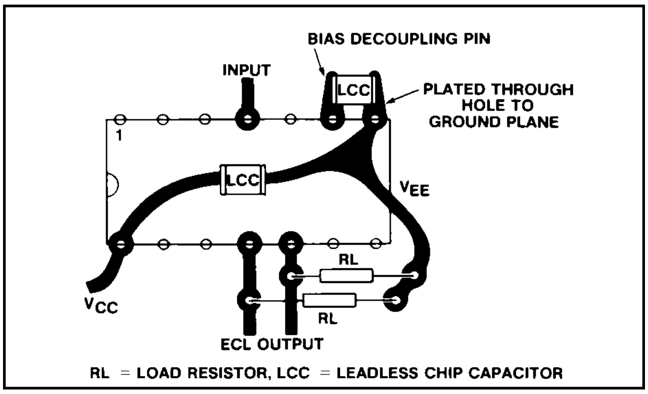

Fig.1 single point grounding

It is well known that the effect of mismatching a transmission line is to cause variations in the voltage along the line. Standard practice at Mitel Semiconductor has been to use a 5:1 attenuator manufactured from ‘microdot’ resistors as an attenuator feeding a 50Ω sampling oscilloscope or a power meter. Although a high VSWR will exist on the line from the generator to the test fixture, the theory is that the line from the power meter to the attenuator will be a matched line, and so the power measured is 14dB lower than the power at the device input pin. This method has been proved very successful, even if simple, and offers some advantages over the use of hybrids or directional couplers.

The use of a matched 50Ω system can help, and using microstrip techniques, a track with a defined impedance is reasonably practical. The impedance of a microstrip line is given by:

$$Zo = 377\ (L/w)\ (1/\varepsilon r)$$

Where L = dielectric thickness, w = width of track and εr is the relative permeability of the board material.
Some correction factors have to be applied, and typically, on 1/16 inch glass fibre epoxy board, the following sizes provide a guide to track width

100Ω- 1mm
76Ω - 2mm
80Ω - 4mm

These impedances rely on the ground plane on the obverse of the board being complete, and where boards are wave soldered, it may be necessary to make arrangements to prevent blistering.

The input level of a divider should be maintained within the guaranteed operating window shown on its data sheet (Fig.2).

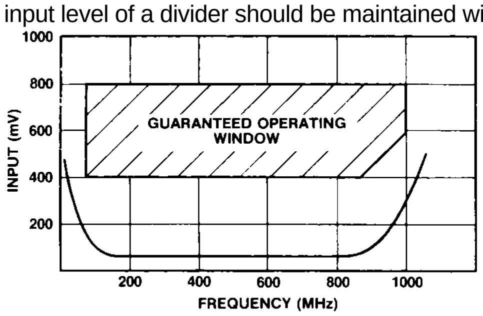

Fig.2 Example of input sensitivity curves

Excessive input can vary in its effects, from causing permanent damage to miscounting, especially when cold. Running the device at too low a level can cause problems, even though the level is within the ‘typical’ performance line of the device An ECL output signal on pin 6 of the device in Fig.3 can couple 60mV of signal to the input shown on Fig.2 at 500MHz. Such a level of coupling can lead to divider jitter if the input signal is low, and it becomes very necessary to keep the inputs and outputs well separated at the higher frequencies. This includes ECL lines to modulus control pins on two modulus dividers.

Most dividers are edge triggered, and although they are specified over a frequency range with sine wave input, they will operate to lower frequencies provided a suitably high slew rate is provided on the input signal. This is generally of the order of 100 to 200 volts/microsecond. This should be achieved by shaping of the input signal, for example by limiting rather than by overdriving the device.

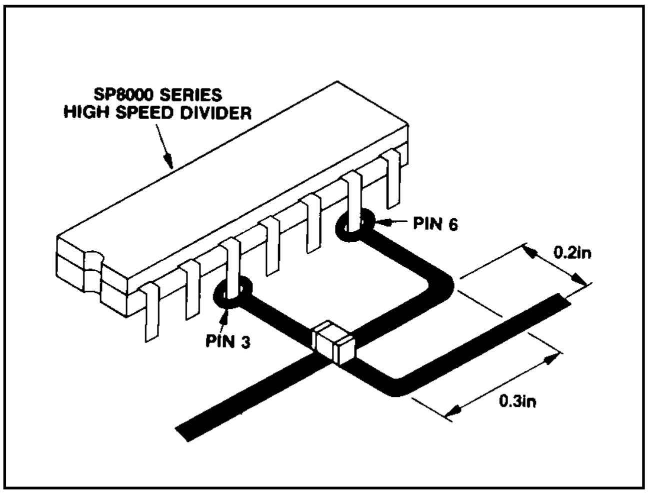

Fig.3 Coupling between parallel tracks

The outputs of devices may be of the following forms:

(1) ECL
(2) Open collector TTL
(3) TTL
(4) CMOS

Of these, the ECL output is well defined; some devices require external load resistors and the data sheet should be consulted. Where these external resistors are required, suitable interconnection techniques should be used between them and the device; the resistors should be carefully chosen for their non-inductive properties when output frequencies are very high. Where an ECL output divider drives another divider it is best to AC couple, since few dividers are strictly ECL compatible on their inputs.

Open collector TTL outputs are relatively slow. Although the negative edge is limited in speed by the turn-on time of the output transistor, the rising edge is limited by the external load resistor and capacitance to ground. In practice this means that short narrow tracks are required to the following device, and a minimum 'fan-in' load provided. In addition, open collector TTL should not be used above about 10MHz output frequency.

True TTL outputs are not so limited, because of the active pull-up. Nevertheless, the use of such outputs at frequencies above about 25-30MHz is not recommended, especially into capactive loads. Loads of more than 30pF should not be d riven faster than about 15MHz. Note that the current drawn by true TTL outputs increases with increasing load capacitance.

CMOS outputs are, on the face of it, TTL-compatible. However, investigation will show that the outputs are not guaranteed to meet TTL levels at TTL currents and it is not recommended that CMOS output devices be used to directly drive TTL. Where an interface of this sort is required, an active transistor interface should be used.

Fig.4 shows a circuit for an ECL-TTL interface, using a line receiver. Simple circuits using one or two transistors cannot be guaranteed to work over all the tolerances of ECL output voltages and temperature ranges.

Interfacing to dividers is not difficult if a few simple rules are obeyed. These are:

(1) Observe the input requirements - guaranteed input operating area, and slew rate.
(2) Do not use open collector outputs above 10MHz.
(3) Do not use CMOS outputs to drive TTL.
(4) Use a sensible layout with good components, and sensible values - 0.1 microfarad ceramic capacitors are NOT bypasses at 1.5GHz.

Treating dividers as RF linear devices is probably the best way to ensure successful applications at high frequencies. There is no magic in HF design, only intelligent layout and sensible component choice.

Impedance Matching

The use of microstrip techniques has been mentioned already. However, in itself this will not produce a matched network and various possibilities exist to improve the matching at the input of a device. These include Tchebycheff impedance transforming networks, narrow band 'L' matching networks, and at high enough frequencies, the use of transmission lines. Wideband matching is often difficult, and attempts should be made to use networks that have the lowest possible working Q. This is for two reasons: firstly a high Q network will not only be narrow band, but will have the capability of increasing the losses, and secondly, a low Q network is generally more tolerant of component variations.

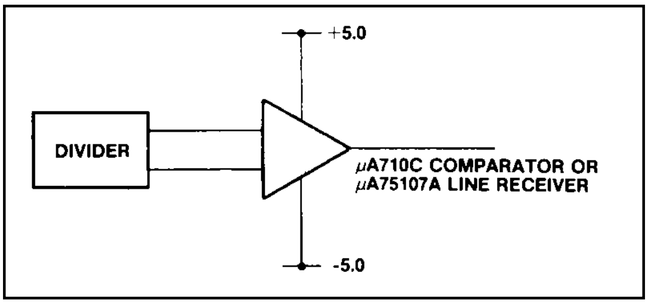

Fig.4 ECL/TTL interface

The greater losses in high Q circuits occur because of the greater circulating current: the loss power is I^2R, so that if the Q is doubled with all else constant, the power loss is increased by 4 times.

The easiest method of determining matching components is by means of the Smith Chart.

THE SMITH CHART

The input impedance of SP8000-series high speed dividers varies as a function of frequency and is therefore specified on the datasheets by means of Smith Charts. The following information is included in this handbook as a guide to their interpretation and use.

Construction of the chart

The chart is constructed with two sets of circles, one set comprising circles of CONSTANT RESISTANCE (Fig. 5) and the other circles of CONSTANT REACTANCE (Fig. 6). The values on these circles are normalised to the characteristic impedances of the system by dividing the actual value of resistance or reactance by the characteristic impedance e.g. in a 50Ω system, a resistance of 100Ω is normalised to a value of 2.0.

By combining Figs. 5 and 6 to form Fig. 7, a chart is produced in which any normalised impedance has a unique position on the chart, and the variation of this impedance with frequency or other parameters may be plotted.

A further series of circles may be plotted on the chart: these are circles of constant VSWR, and represent the degree of mismatch in a system. The VSWR is the ratio of the device impedance to the characteristic impedance, and is always expressed as a ratio greater than 1: thus a 25Ω device in a 50Ω system gives rise to a 2:1 VSWR. These circles of constant VSWR have been added in Fig. 7.

Any point can be represented on the Smith Chart: for example an impedance of 150-*j*75Ω can be represented by a normalised impedance (in a 50Ω system) of 3-*j*1.5 and this point is plotted in Fig. 7 as point A.

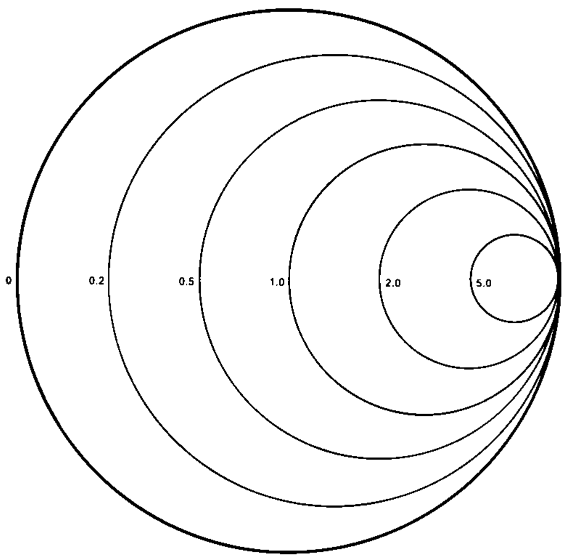

Fig.5 Constant resistance circles

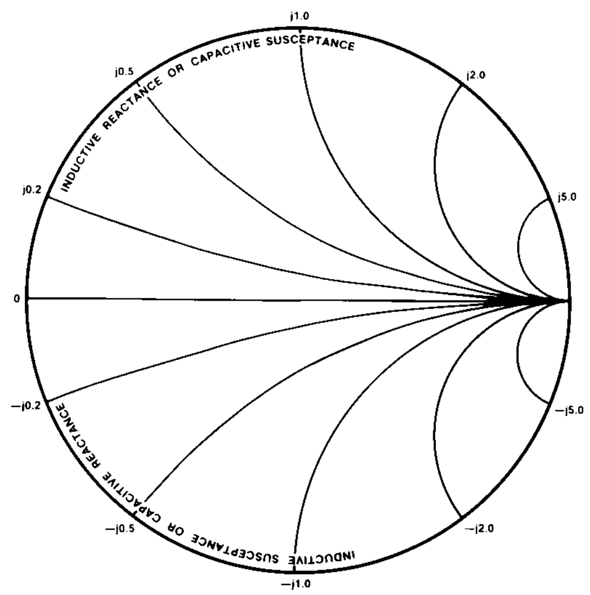

Fig.6 Constant reactance cirles

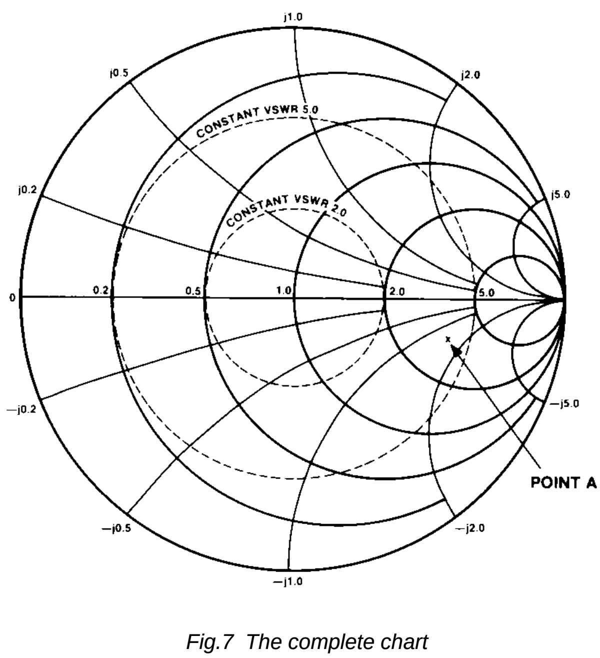

Fig.7 The complete chart

Network calculations

The main application for Smith Charts with integrated circuits is in the design of matching networks. Although these can be calculated by use of the series to parallel (and vice-versa) transforms, followed by the application of Kirchoff's Laws, the method can be laborious. Although the Smith Chart as a graphical method cannot necessarily compete in terms of overall accuracy, it is nevertheless more than adequate for the majority of problems, especially when the errors inherent in practical components are taken into account.

Any impedance can be represented at a fixed frequency by a shunt conductance and susceptance (impedances as series reactance and resistance in this context). By transferring a point on the Smith Chart to a point at the same diameter but 180° away, this transformation is automatically made (see Fig. 8) where A and B are the series and parallel equivalents.

It is often easier to change a series RC network to its equivalent parallel network for calculation purposes. This is because as a parallel network of admittances, a shunt admittance can be directly added, rather than the tortuous calculations necessary if the series form is used. Similar arguments apply to parallel networks, so in general it is best to deal with admittances for shunt components and reactances for series components.

Admittances and impedances can be easily added on the Smith Chart (see Fig. 9) Where a series inductance is to be added to an admittance (i.e parallel R and C), the admittance should be turned into a series impedance by the method outlined above and in Fig 8. The series inductance can then be added as in Fig. 9 (see also Fig. 10).

Point A is the starting admittance consisting of a shunt capacitance and resistance The equivalent capacitive impedance is shown at point B. The addition of a series inductor moves the impedance to point C. The value of this inductor is defined by the length of the arc BC, and in Fig. 10 is -*j*0.5 to *j*0.43 i.e. a total of *j*0.93. This reactance must of course be denormalised before evaluation. Point C represents an inductive impedance which is equivalent to the admittance shown at Point D. The addition of shunt reactance moves the input admittance to the centre of the chart, and has a value of *j*2.0 Point D should be chosen such that it lies on unity impedance/conductance circle: thus a locus of points for point C exists.

This procedure allows for design of the matching at any one frequency. Wide band matching is more difficult and other techniques are needed. Of these, one of the most powerful is to absorb the reactance into a low pass filter form of ladder network: if the values are suitably chosen, the resulting input impedance is dependent upon the reflection coefficient of the filter.

At frequencies above about 400MHz, it becomes practical to use sections of transmission line to provide the necessary reactances, and reference to one of the standard works on the subject is recommended.

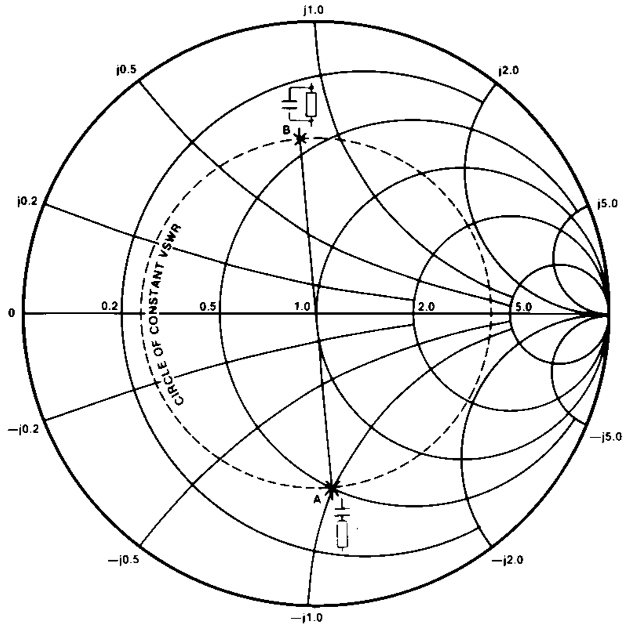

Fig.8 Series reactance to parallel admittance conversion

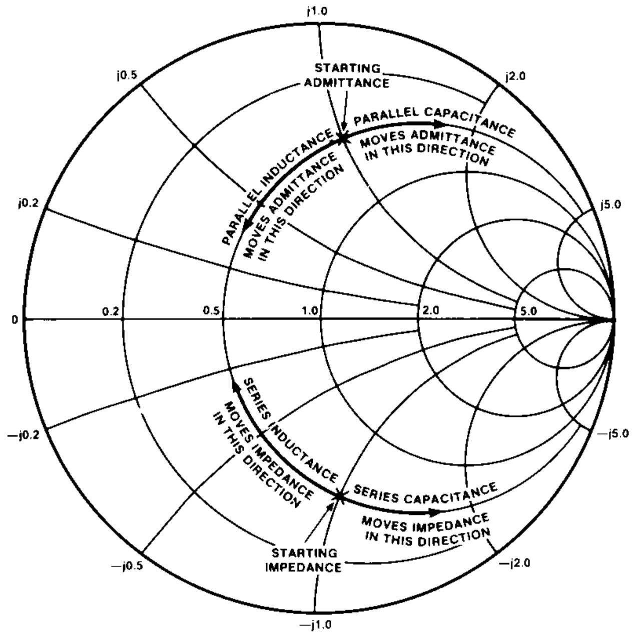

Fig.9 Effects of series and shunt reactance

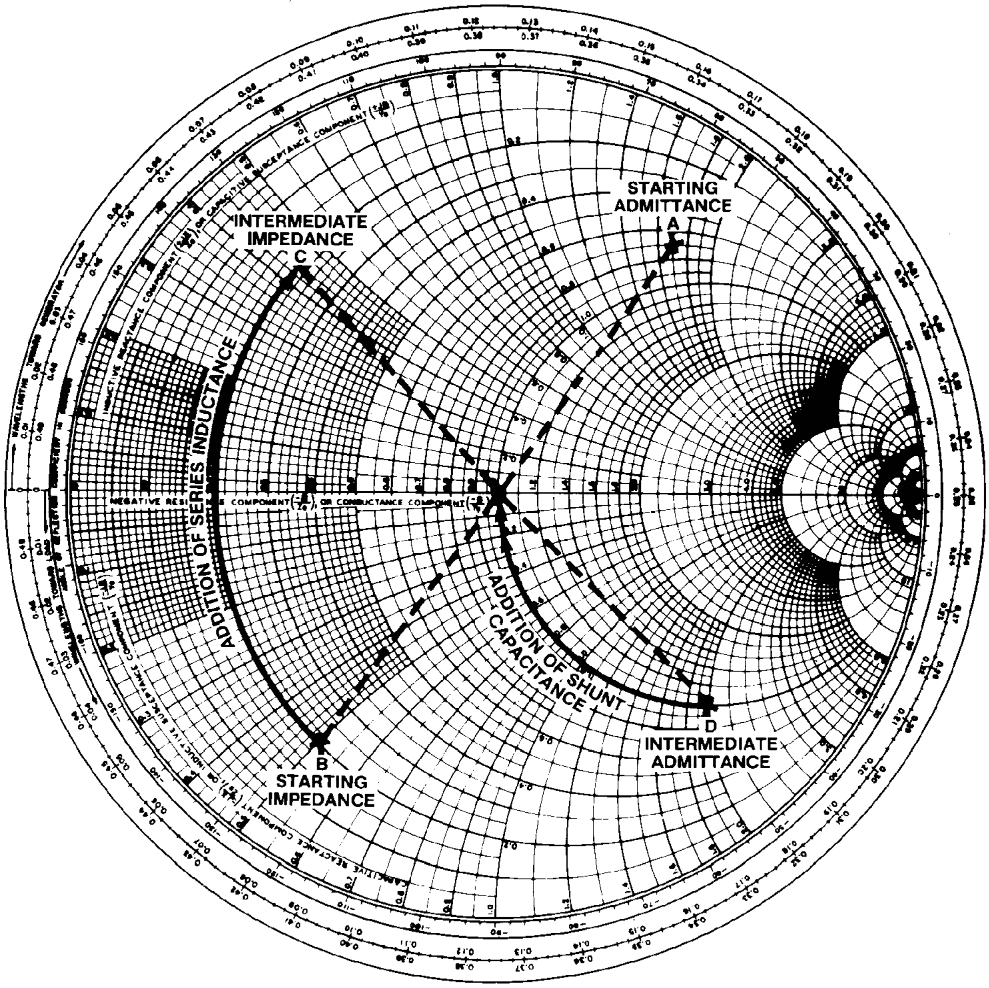

Fig.10 Matching design using the Smith Chart

PHASE NOISE AND DIVIDERS

Phase noise is becoming increasingly important in systems and it is necessary to minimise its effects. First, however, phase noise must be defined.

A spectrally pure signal of a given frequencywould appear on a perfect spectrum analyser display as a single straight line as in Fig 11. If the signal is frequency modulated with a discrete modulation frequency, the result will be a comb of frequencies as in Fig.12, while modulation with noise will produce an output spectrum as in Fig.13. Note that the noise density decreases as the offset from the carrier increases. This effect is the result of the effectively lower modulation index *m.* In the case of a Voltage Controlled Oscillator modulated by white noise, a similar effect will be seen, because for a given deviation f, the modulation index *m, (= 1/fmod) is* greater for lower frequencies than for higher frequencies. Thus the number of sidebands is greater for lower frequencies, and the noise spectral density increases as the carrier is approached.

The causes of phase noise in dividers are not well understood, but the effects of internal noise on the switching point of the various flip-flops cannot be ignored The 1/f noise will obviously inter-relate to the phase noise if this is so, and it is interesting to note that various measurements of Gallium Arsenide dividers suggest performances 20 to 30dB worse than for ECL dividers. Rohde (ref.4) suggests that TTL and CMOS are much better than ECL, although little work has been published in this field, possibly because of the measurement difficulties.

The non-saturating nature of ECL, the fact that the transistors are designed and processed for high speed rather than low noise, and the smaller signal swings than TTL or CMOS, lead intuitively to the conclusion that ECL should be worse than either of these other two logic families. This appears to be the case, while the high 1/f noise knee of Gallium Arsenide devices leads to the high relatively close in phase noise.

Devices with slow output edges, such as open collector TTL output stages may also be expected to be worse, which is again born out in practice.

Minimisation of phase noise requires the use of well filtered supplies, correct input levels and minimisation of noise in level changing circuitry.

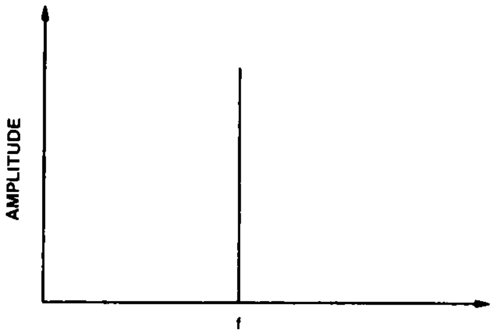

Fig.11 Spectrally pure signal

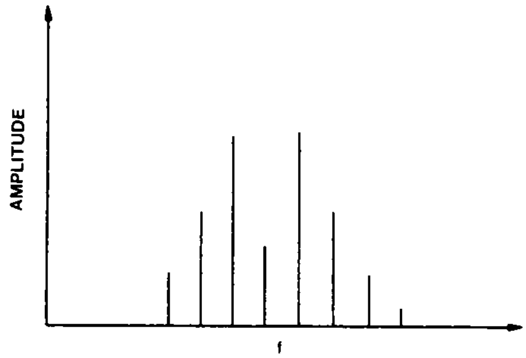

Fig.12 Spectrally pure signal, frequency modulated with single tone

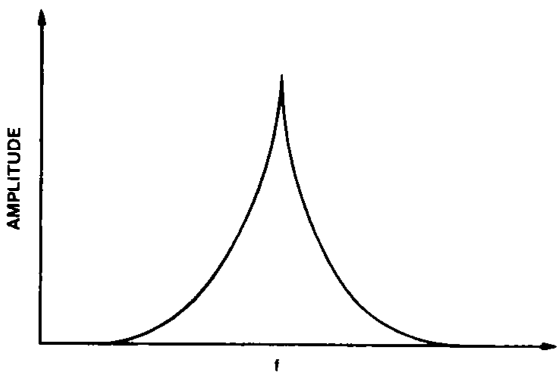

Fig.13 Spectrally pure signal, frequency modulated by noise

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